大葉大學 97 學年度　研究所碩士班　招生考試試題紙

系　所　別	組　別	考　試　科　目 （中　文　名　稱）	考　試 日　期	節　次	備　　註
電機工程學系碩士班	乙組	控制系統	4 月 13 日	第　二　節	共二頁

註：考生可否攜帶計算機或其他資料作答，請在備註欄註明（如未註明，一律不准攜帶） 10:40~12:10　P2-1

✕ 控制系統或計算機概論（只能選擇一考科作答，不可跨考科作答）

1. Please give the following definition (20%)
   (1) Control system (4%)
   (2) Linear time-invariant system (4%)
   (3) Transfer function (4%)
   (4) Gain margin and phase margin (4%)
   (5) Minimum-phase system (4%)

2. Consider a DC motor shown as follows. Given the torque constant K_i, the back-emf constant K_b, the rotor inertia J, and viscous-friction coefficient B, please find
   (1) The block diagram of the DC-motor system. (10%)
   (2) The transfer function of the DC-motor system between the motor displacement θ and the input voltage e_a. (10%)

3. Given the following control system:

   Please (1) sketch its root locus (10%); (2) find the range of K such that the system is stable. (10%)

4. Consider a closed-loop system as shown below, where $K=32$ and $G(s) = \dfrac{(1+2s)}{s(2+s)(s+8)}$. Please draw its

   Bode plot. (20%)

5. Given the state matrix $A = \begin{bmatrix} 0 & 1 \\ -8 & -6 \end{bmatrix}$, find its state transition matrix $\phi(t) = e^{At}$. (20%)

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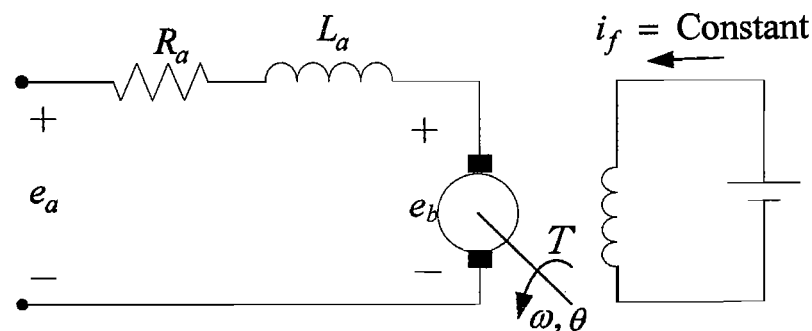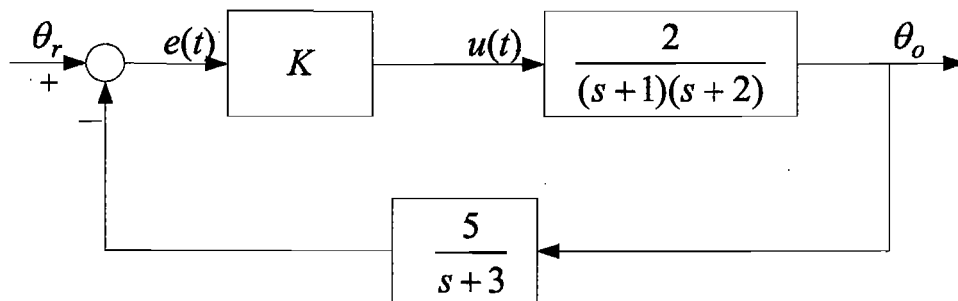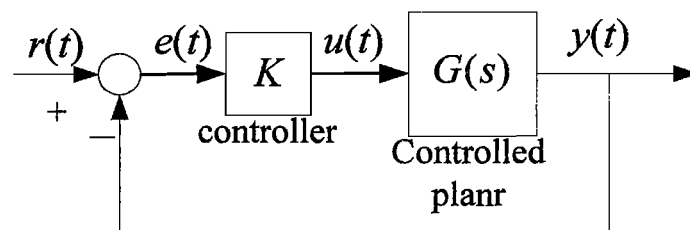| 系　所　別	組　別	考　試　科　目 （中　文　名　稱）	考　試 日　期	節　次	備　　註
電機工程學系碩士班	乙組	計算機概論	4 月 13 日	第 二 節	共二頁

註：考生可否攜帶計算機或其他資料作答，請在備註欄註明（如未註明，一律不准攜帶）(0240u1210　p2-2

6. Please give the following definition (20%)　　※控制系統或計算機概論（只能選擇一考科作答，不可跨考科作答）
　　(1) Algorithm and program (4%)
　　(2) Source code, object code, and machine code (4%)
　　(3) Global variable and local variable (4%)
　　(4) Direct addressing and indirect addressing (4%)
　　(5) Interpreter and compiler (4%)

7. Given the Fibonacci number described as follows.
　　$f(n) = f(n-1) + f(n-2), \ f(0) = f(1) = 1$
　　Please use your familiar programming language to code a program to generate the value. (20%)

8. Please explain the methods of search algorithm (10%) and assess their average time to search an object in *n* objects. (10%)

9. Please code a program to calculate *n*! using a recursive subprogram. (20%)

10. Please design a 4-bit adder/subtractor using digital logic circuit. (20%).