註：考生可否攜帶計算機或其他資料作答，請在備註欄註明（如未註明，一律不准攜帶）

＊　計算題答案應詳列計算步驟，否則一概不予計分。

＊　可使用計算機。　　　　　　　　　　　　　　　　P2-1

＊　本試題共二頁。

一、單選選擇題：

(27%，每題 3%，答錯倒扣 1%，未答不扣分，答案卷上須按題目順序答題，否則不予計分)

1. By increasing the reverse bias voltage of a pn junction diode (before breakdown), the junction capacitance will (A) decrease (B) increase (C) increase first, then decrease (D) decrease first, then increase.

2. Which one of the following is true for an ideal op amp? (A) $R_{in} = 0$ and $R_{out} = 0$ (B) $R_{in} = \infty$ and $R_{out} = 0$ (C) $R_{in} = 0$ and $R_{out} = \infty$ (D) $R_{in} = \infty$ and $R_{out} = \infty$.

3. In the following feedback topologies, which one can increase the input resistance and increase the output resistance? (A) shunt-series (B) series-shunt (C) shunt-shunt (D) series-series.

4. Which one of the following is NOT an advantage of negative feedback? (A) Extend the bandwidth, (B) Reduce nonlinear distortion, (C) Desensitize the gain, (D) Increase the gain.

5. Which one of the following statements is NOT true? (A) The common-emitter configuration suffers from the Miller effect. (B) The cascode configuration consists of a common-source transistor followed by a common-base transistor. (C) The Class A power amplifier suffers from crossover distortion. (D) For the feedback amplifier to be stable, its pole must all be in the left half of the s plane.

6. The highest power conversion efficiency of a Class B power amplifier is (A) 0% (B) 25% (C) 50% (D) 78.5%.

7. Which one is the fastest logic circuit family? (A) NMOS (B) PMOS (C) TTL (D) ECL.

8. For a BJT operated at room temperature, the collector current is 1mA. Its g_m is: (A) 25m/Ω (B) 40m/Ω (C) 25 mV (D) 40Ω.

9. Which one of the following statements is NOT true? (A) Zener diodes operate in the breakdown region. (B) The Early effect will result in a decrease in the effective base width. (C) Early effect will result in decrease in the collector current. (D) The emitter follower is useful as a voltage buffer.

二、計算題：(73%)

1. An alternative bridge amplifier configuration with high input resistance is shown in Fig-1.

    (a) (5%) What is the gain V_o/V_I?

    (b) (5%) For op amps using ±15V supplies that limit at ±13V, what is the largest sine wave you can provide across R_L?

    (c) (5%) Using 2 kΩ as the smallest resistor, find resistor values that make V_o/V_I = 10 V/V.

2. The MOSFETs in the circuit of Fig-2 are matched, with $k_n'(W/L)_1 = k_p'(W/L)_2 = 100$ μA/V^2 and $|V_t|$ = 2V. The resistance R = 10MΩ.

    (a) (5%) For G and D open, what are the drain currents I_{D1} and I_{D2}?

    (b) (5%) For finite r_o ($r_o = |V_A| / I_D$, $|V_A|$ = 200V), what is the voltage gain from G to D and the input resistance at G?

    (c) (5%) If G is driven through a large coupling capacitor from a source V_i having a resistance of 1MΩ, find the voltage gain V_d/V_i.

    (d) (5%) For what range of output signals do Q1 and Q2 remain in the pinch-off region?

大葉大學 九十四 學年度　研究所碩士班　招生考試試題紙

系　所　別	組　別	考　試　科　目 （中　文　名　稱）	考　試 日　期	節　次	備　　註
電機工程學系碩士班 電信工程學系碩士班	甲、乙組	電子學	3 月 27 日	第　二　節 10:30～12:00	

註：考生可否攜帶計算機或其他資料作答，請在備註欄註明（如未註明，一律不准攜帶）

P2-2

3. (12%) For the circuit shown in Fig-3, utilize the constant-voltage drop model (0.7V) for each conducting diode and sketch the transfer characteristics V_o-V_I of the circuit.

4. (6%) A BJT for which $\beta_F = 100$ and $\alpha_R = 0.2$ operates with a constant base current but with the collector open. What value of V_{CEsat} would you measure?

5. Sketch the Bode magnitude and phase plots for the following functions:

(a) $T(s) = \dfrac{100s}{(s+100)(s+100000)}$　(10%)
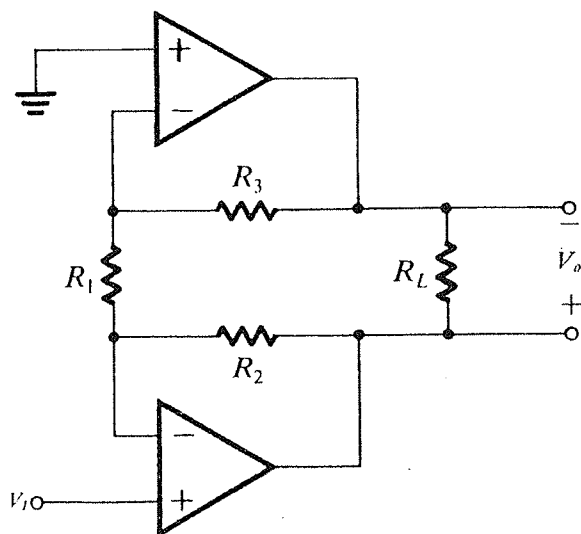
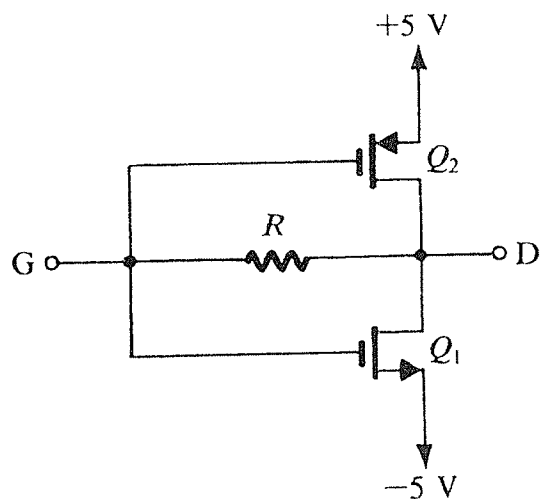(b) $T(s) = \dfrac{10^5(10^5+s)}{(10^3+s)(10^4+s)}$　(10%)

Fig-1

Fig-2
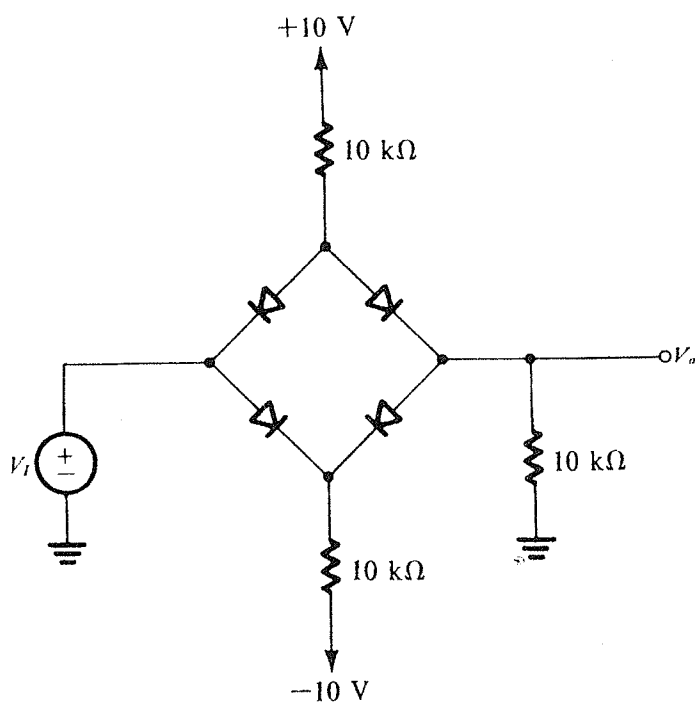

Fig-3