| 大葉大學 九十三 學年度 研究所碩士班 招生考試試題紙 | | | | | |
|---|---|---|---|---|---|
| 系 所 別 | 組 別 | 考 試 科 目<br>(中 文 名 稱) | 考 試<br>日 期 | 節 次 | 備 註 |
| 電機工程學系 | 乙組 | 系統理論 | 3月28日 | 第3 節 | P-1<br>共二頁 |

註：考生可否攜帶計算機或其他資料作答，請在備註欄註明（如未註明，一律不准攜帶） 13:30～15:00

注意事項

1、考題共十題可任選五題作答，每題20分。不得超過五題作答，只前五題算分。只能選大題，不可選小題。

2、標明題號依序作題。

3、可以使用尺、量角器及不可程式之計算機(Calculator)。

1. Explain the following terms: (20%)
   (a) Superscalar processing
   (b) Computer virus
   (c) Cache miss
   (d) Non-preemptive CPU scheduling

2. A system has four inputs, $W, X, Y, Z$ and two outputs, $F$ and $G$,
   $F(W, X, Y, Z) = \Sigma m(5, 8, 9, 12, 13)$
   $G(W, X, Y, Z) = \Sigma m(1, 3, 5, 8, 9, 11)$
   (a) Implement the system with a two-level NAND circuit. (simplified sum of products solution needed) (10%)
   (b) Implement the system with a Programmable Logic Arrays (PLA) using no more than four different terms. (10%)

3. Design a synchronous counter that goes through the sequence 0 4 2 1 6 and repeat using *JK* flip flops. Show the state table, the *K*- maps and equations for the flip flop inputs, and the logic circuit diagram. (20%)

4. (a) Write a bubble sort program using C language for performing the sort of $n$ integers in ascending order. (10%)
   (b) Considering the integer sequence : $5^*$, 7, 4, $5^+$, 3 (here $5^*$ and $5^+$ mean the value of 5, and * and + just indicate the positions of two 5s in the initial sequence), sort the above sequence in ascending order with bubble sort method. What is the final sequence after sorting and how many data exchange are performed in whole sorting process. (10%)

5. (a) Explain the Fetch-Decode-Execute machine cycle of a CPU in detail. (10%)
   (b) The two designs for CPU architecture are CISC and RISC. Compare and contrast CISC with RISC. If pipelining technique is applied, which CPU architecture is more efficient in executing program instructions ? Explain your answer in detail. (10%)

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| 電機工程學系 | 乙組 | 系統理論 | 3月28日 | 第 3 節 | P-2 共二頁 |

註：考生可否攜帶計算機或其他資料作答，請在備註欄註明（如未註明，一律不准攜帶） 13:30 ~ 15:00

(20%)6. Find the transfer function, $V_o(s)/V_i(s)$, for the circuit given in Figure 6.

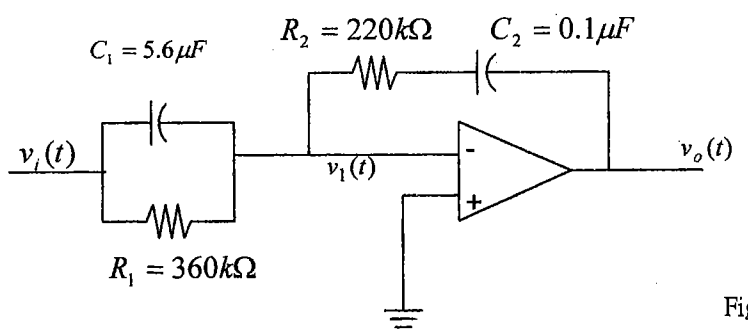


Figure 6

(20%)7. Find the state-space representation in phase-variable form for the transfer function shown in Figure 7 and draw its block diagram based on the state equations.


Figure 7

(20%)8. Sketch the root locus for the system shown in Figure 8.

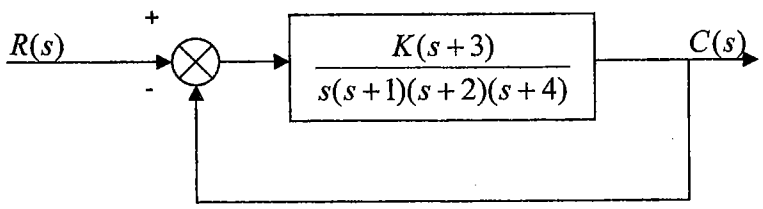


Figure 8

(20%)9. Determine whether the system

$$\dot{x} = Ax + Bu = \begin{bmatrix} -1 & 1 & 2 \\ 0 & -1 & 5 \\ 0 & 3 & -4 \end{bmatrix} x + \begin{bmatrix} 2 \\ 1 \\ 1 \end{bmatrix} u$$

is controllable. why ?

(20%)10. Given the function in Eq. (10.1), find the sampled time function.

$$F(z) = \frac{0.5z}{(z-0.5)(z-0.7)} \qquad \text{Eq. (10.1)}$$