

系所別	組別	考試科目 (中文名稱)	考試日期	節次	備註
電機所博士班	乙組	系統理論	6月21日	第一節	可帶計算機

註：考生可否攜帶計算機或其他資料作答，請在備註欄註明（如未註明，一律不准攜帶）

註1:考生可由下列十題中,任選五題作答,超過五題部份不予計分.

1. Answer the following Digital Design questions.

- (a) Construct a 5-to-32-line decoder with four 3-to-8-line decoders with enable and a 2-to-4-line decoder. Use block diagrams for the components. (6%)
- (b) Implement the following Boolean function with a 4 × 1 multiplexer and external gates. (8%)

$$F(A, B, C, D) = \sum m(1, 3, 4, 11, 12, 13, 14, 15)$$

- (c) A combinational circuit is defined by the following three Boolean functions:

$$F_1 = \bar{x} \bar{y} \bar{z} + xz$$

$$F_2 = x \bar{y} \bar{z} + \bar{x}y$$

$$F_3 = \bar{x} \bar{y} z + xy$$

Design the circuit with a decoder and external gates. (6%)

2. Answer the following Internal Memory questions.

- (a) The cache size, mapping function, replacement algorithm, and write policy are basic design elements that serve to classify and differentiate cache architectures. Please list two kinds of mapping functions, replacement algorithms and write policies, respectively. (6%)
- (b) Design a 16-bit memory of total capacity 8192 bits using SRAM chips of size 64 × 1 bit. Give the array configuration of the chips on the memory board, showing all required input and output signals for assigning this memory to the lowest address space. The design should allow for both 8-bit and 16-bit word accesses. (14%)

3. Answer the following Algorithm and Data Structure questions.

- (a) Using O -notation, the time-complexity of an algorithm can be described. Give the mathematical definition of O -notation. (5%)
- (b) List the following three time-complexity functions in increasing order as n becomes very large. (5%)

$$(1.01)^n, 10^{\log n}, n^{0.001n}$$

- (c) Draw the internal memory representation of a full binary tree of depth 3 using (i) sequential array and (ii) linked representations. (5%)
- (d) *Inorder*, *preorder*, and *postorder* are three types of binary tree traversals. Write three recursive procedures for describing these three traversals, respectively. (5%)

- 4. For the state equation and initial state vector shown in Eqs.(1), where $u(t)$ is a unit step, find the state-transition matrix and then solve for $x(t)$.(20%)

系所別	組別	考試科目 (中文名稱)	考試日期	節次	備註
電機所博士班	乙組	系統理論	6月21日	第一節	可帶計算機

註：考生可否攜帶計算機或其他資料作答，請在備註欄註明（如未註明，一律不准攜帶）

$$\dot{x}(t) = \begin{bmatrix} 0 & 1 \\ -8 & -6 \end{bmatrix} x(t) + \begin{bmatrix} 0 \\ 1 \end{bmatrix} u(t) \quad (1)$$

$$x(0) = \begin{bmatrix} 1 \\ 0 \end{bmatrix}$$

5. Given the system represented in state space by Eqs.(2),

$$\dot{x} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ -2 & -5 & -7 \end{bmatrix} x + \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix} u \quad (2)$$

$$y = [1 \ 0 \ 0]x$$

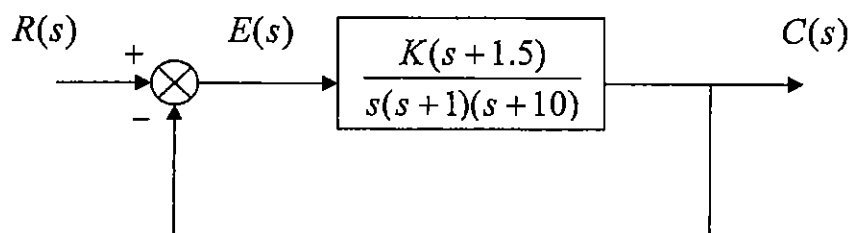
transform the system to a new set of state variables, z, where the new state variables are related to the original state variables, x, as follows:

$$\begin{aligned} z_1 &= 2x_1 \\ z_2 &= 3x_1 + 2x_2 \\ z_3 &= x_1 + 4x_2 + 5x_3 \end{aligned} \quad (20\%)$$

6. Evaluate the steady-state error for the system described by Eqs.(3). for unit step and unit ramp inputs. Use the final value theorem.(20%)

$$A = \begin{bmatrix} -5 & 1 & 0 \\ 0 & -2 & 1 \\ 20 & -10 & 1 \end{bmatrix}; \quad B = \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix}; \quad C = [1 \ 1 \ 0] \quad (3)$$

7. Consider the system shown in Figure. Design the value of gain, K, to yield 1.52% overshoot. Also estimate the settling time, peak time, and steady-state error.(20%)



8. 說明太陽能電池之BSF(Back Surface Field)構造及其優點.(20%)

9. 說明太陽能電池之最大功追蹤之增量電導法及其優缺點.(20%)

10. 敘述充電方式之二階段充電法及三階段充電法並說明其優點.(20%)