A 0.6-V MOSFET-Only Subthreshold-Leakage Suppressed CMOS Fully Differential Switched-Capacitor Amplifier

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ABSTRACT

This paper presents a 0.6-V MOSFET-only subthreshold-leakage suppressed CMOS fully differential switched-capacitor amplifier with an analog T-switch scheme. The circuit uses substrate-biased MOSFETs in its depletion region as capacitors linearized by a compensation technique. The circuit design of major building blocks is described herein. The experimental results demonstrate the performance of this circuit. The switched-capacitor amplifier operates with a signal-to-total harmonic distortion ratio of 36 dB for an input 10-kHz sinusoidal amplitude of 0.12 Vpp and dissipates 145.39 μW. The circuit was fabricated in a standard 0.18 μm CMOS technology with an area of 500 μm× 520 μm. The experimental results confirm the capability of compensated depletion-mode MOS capacitors and the proposed analog T-switch scheme to fulfill circuit requirements.

Keywords: MOSFET-only, subthreshold leakage, low voltage, CMOS, switched-capacitor amplifier.

一 0.6-伏特只用金氧半場效電晶體次臨界-洩漏壓抑互補金氧半完全差動交換電容放大器

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摘　要

本論文提出一 0.6-伏特只用金氧半場效電晶體互補金氧半完全差動次臨界洩漏壓抑低電壓交換電容放大器，並採用類比 T-開關。本電路使用了基板偏壓的金氧半場效電晶體工作在空乏

區以用來作為電容使用。詳細的電路在本文中被清楚的描述。此交換電容放大器運作於一輸入

10kHz 振幅 0.12 Vpp 正弦信號，信號-對-全部諧波失真比可達 36 dB，且消耗 145.39- μ W。此電

路以標準 TSMC 0.18um CMOS 製程製作且其面積是 500 μ m ×520 μ m。實驗結果及實體佈局結果

證實了本設計的可行性，並滿足了本設計的需求。

關鍵詞：只用金氧半場效電晶體，次臨界洩漏壓抑，低電壓，互補金氧半，交換電容放大器。

I. INTRODUCTION

Analog signal amplification in discrete-time system can be performed by switched-capacitor amplifiers [7]. Switched-capacitor (SC) amplifier has been used in the design of digital-to-analog converter [16]. The schematic for the switched-capacitor amplifier is shown in Fig.1. The phase signals ϕ_1 (ϕ_1') and ϕ_2 (ϕ_2') are ono-overlapping. ϕ_1' (ϕ_2') is advanced slightly, compared to ϕ_1 (ϕ_2). Assuming an infinite operational amplifier (op amp) gain, the output voltage at the end of ϕ_2 is given by

$$V_{out}(nT) = \frac{C_1}{C_2} V_{in}(nT - \frac{T}{2})' \tag{1}$$

irrespective of the op amp offset voltage. If the clock waveforms shown in parentheses are used, then an inverting function is realized, and

$$V_{out}(nT) = -\frac{C_1}{C_2} V_{in}(nT)' \tag{2}$$

again independent of the op amp input offset voltage. During the reset phase (ϕ_1), C_3 is connected in feedback around the op amp which causes the output to change only by the op amp input offset voltage. The switches are realized as CMOS transmission gates. For low supply voltages, a conductance gap begins to appear around the middle of the supply range [2]. This means that under low-voltage operation, this configuration no longer works. Several low-voltage switched-capacitor amplifiers have been reported, but all are implemented in a high-threshold voltage (high-V_{th}) process [4, 17]. Previous works mainly tackled the realization of low-voltage analog
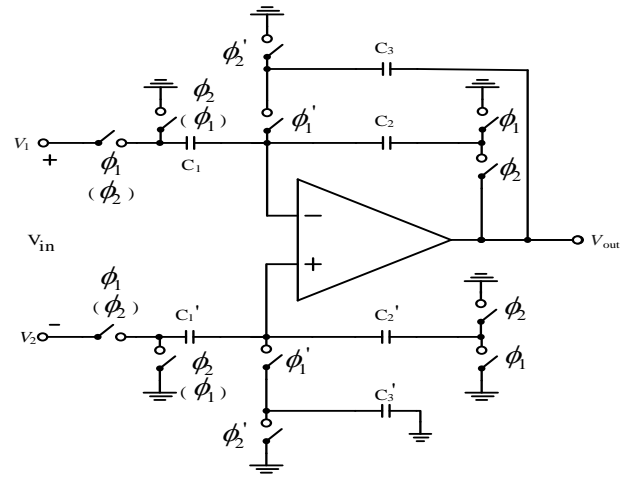

Fig. 1. A CMOS differential-to-single-ended SC amplifier. Depending on the input-stage clock signals, the amplifier can be either noninverting (as shown) or inverting (input-stage clocks shown in parentheses).

circuits using high-V_{th} devices, and consequently the issue in charge-based analog circuits was high resistance of MOS switches. To reduce on-state resistance, gates of MOS switches are widened or higher voltages are applied by bootstrap [4].

While moving into ultra-deep submicron CMOS technologies, for low-voltage low-power designs, certain advantages can be gained. On the other hand, some disadvantages also exist. Limited by the transistor breakdown voltage, the rated supply voltage is low in ultra-deep-submicrom CMOS technologies. As a result, the threshold voltage of the transistor is also low, which is advantageous to implement low-voltage applications. With ultra-deep-submicron technologies, the threshold is reduced as the supply voltage is decreased. This makes the driving of the switches possible without bootstrapping circuit. Low-V_{th} devices relax designs of low-voltage operation. In the low-V_{th} process, however, nonlinear subthreshold leakage current can

be a critical issue on analog circuit. There are two ways of reducing the leakage current without significantly increasing the length of a transistor, which will unacceptably increase the on-resistance of the switch [4, 9]. The authors have presented a subthreshold-leakage suppressed 0.6-V CMOS fully differential SC amplifier [6] based on analog T-switch (AT-switch) scheme [4]. In the SC amplifier [6], the operating supply voltage is lower than that of the realizations in [17] and [5], and its signal-to-THD (total harmonic distortion) ratio is higher than that of the realization in [7] and lower than that of the realizations in [17] and [5] because of lower supply voltage.

In integrated analog applications linear capacitors with high capacitance per unit area are desirable. To realize such capacitors extra process layers are needed which increase the cost of fabrication. Recently, several attempts have been done to use gate-to-bulk capacitance of a MOSFET as a capacitor. MOS capacitors (MOSCAP) have large capacitance per unit area because their gate oxide is thin. The main disadvantage of such MOS capacitor is their large voltage dependence caused by different charge distributions in the accumulation, depletion and inversion region. There are several ways of using a MOSFET-based capacitor [11, 13-14, 17]. The device may be in a well or in the substrate. Also, the channel may be created by accumulation or by strong inversion. To realize floating capacitors, the well-embedded device is usually chosen. MOS capacitors biased in the strong inversion or accumulation region are described in [17]. In this work, the necessary bias is realized by a switched dc voltage. However, the required bias voltage is too high for low voltage analog circuits and the need of a switched bias limits the use of SC circuits. A new approach is investigated using MOS capacitor with series and parallel compensation in the depletion region [11, 13-14]. Substrate biasing [11, 13-14] produces a depletion region broading caused by the body effect, which leads to an extension of the linear range of the resulting capacitance. Serial compensation and parallel compensation depletion mode techniques are two commonly used solutions found. Serial compensation combines good linearity with moderate area efficiency. Parallel compensation provides moderate linearity at high area efficiency.

This paper describes the design of a 0.6-V subthreshold-leakage suppressed CMOS fully differential switched-capacitor amplifier (S-LSCFDSCA) in a standard 0.18 μ m CMOS technology using AT-switch scheme. All capacitors are realized using compensated MOSFET operated in the depletion region. In section II an overview of MOSCAP compensation methods is presented. In section III, the circuit realization of this SC amplifier is addressed. Experimental results are presented in section IV to support the ideas put forth in this paper. The conclusion is given in section V

II. COMPENSATED MOS CAPACITORS

As mentioned earlier, nonlinearities of depletion mode MOS capacitor can be eliminated to some extent by antiserial or antiparallel connections of two capacitors. Fig. 2(a) shows the principle diagram of a series compensated depletion mode MOS capacitor (SCDM-MOSCAP). Fig. 2(b) also shows that the linearization with different substrate bias voltages $V_{SB1} = V_{SB2} = V_{SB}$ results in approximately equal specific capacitance values with different usable voltages. This permits a modification of the circuit diagram shown in Fig. 2(a) into an arrangement without floating dc voltage sources (Fig. 2(c)). To realize a high-resistance element between gate node C and analog ground potential $GNDA$ to prevent a gate charging, it is possible to use, e.g. an n-channel MOSFET ($M3$), operated in the subthreshold region.

The principle diagram of a parallel compensated depletion mode MOS capacitor (PCDM-MOSCAP) is shown in Fig. 3(a). Fig. 3(b) also depicts that linearization with different floating substrate bias voltages $V_{SB1} = V_{SB2} = V_{SB}$ results in approximately equal specific capacitance values with different usable voltages. A modification of the circuit diagram shown in Fig. 3(a) into an arrangement without floating dc voltage sources (Fig. 3(c)) is permitted.

Comparing the two methods, it is seen that more area efficient parallel compensated depletion mode MOS capacitors (PCDM-MOSCAPs) have less linearity than the serial depletion mode MOS capacitors (SCDM-MOSCAPs). In both cases usable voltage range can be broaden by applying an additional source bulk voltage
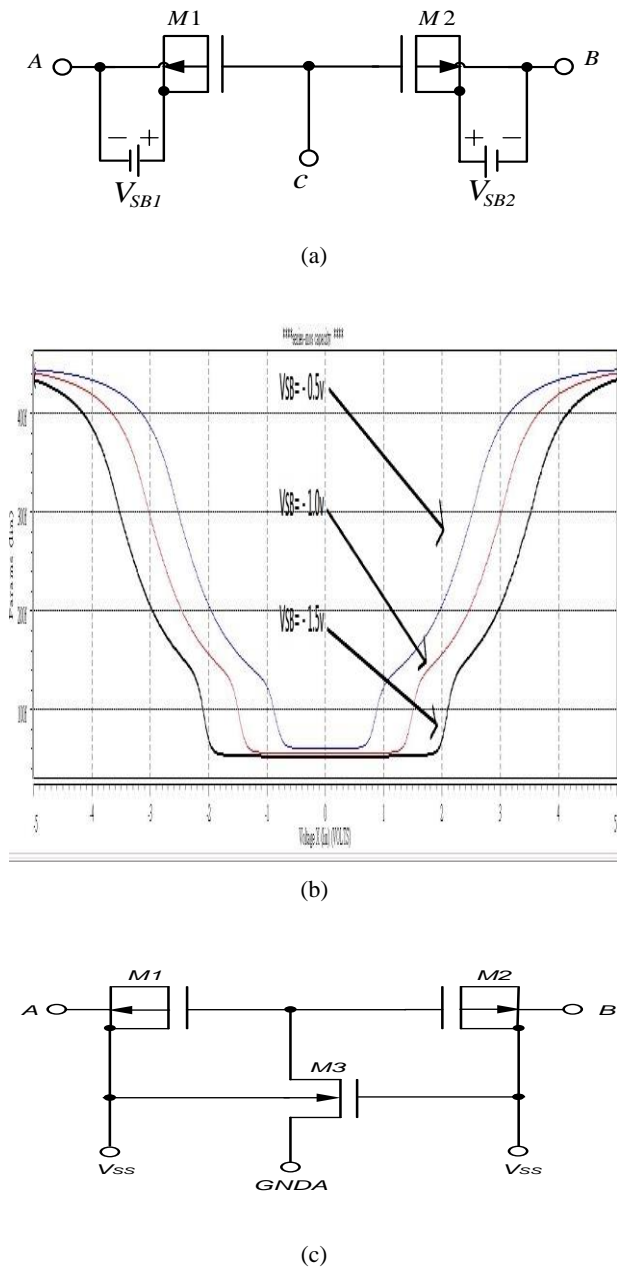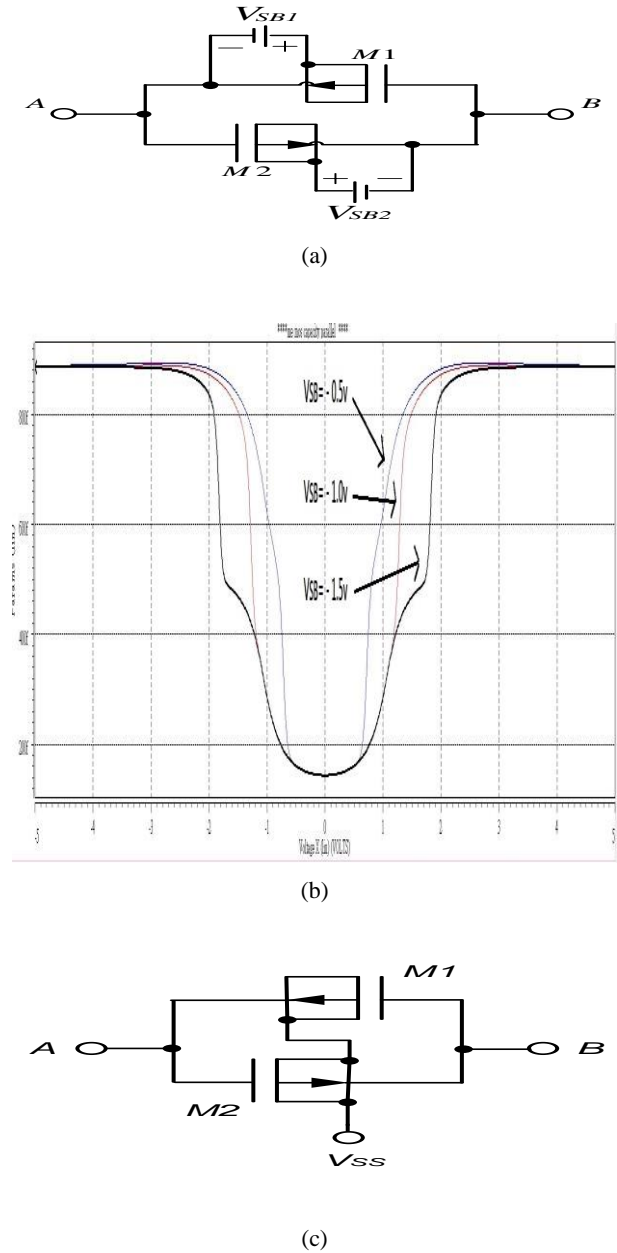
(a)

(b)

(c)

Fig. 2. Series compensated depletion mode MOS capacitor (SCDM-MOSCAP)：(a) principle diagram, (b) simulated *CV* **characteristics (0.18-µm CMOS,** $W_1 = W_2 = 10µm$, **and** $L_1 = L_2 = 10µm$**), and (c) SCDM-MOSCAP with fixed substrate bias and high-resistance element.**

(a)

(b)

(c)

Fig. 3. Parallel compensated depletion mode MOS capacitor (PCDM-MOSCAP): (a) principle diagram, (b) simulated *CV* **characteristics (0.18-µm CMOS,** $W_1 = W_2 = 10µm$, **and** $L_1 = L_2 = 10µm$**), and (c) PCDM-MOSCAP with fixed substrate bias.**

III. CIRCUIT DESCRIPTION

Fig.4 shows the MOSFET-only S-LSCFDSCA, where switches S1_AT and S4_AT (S1'_AT and S4'_AT) are AT-switch's, switches S2_S and S3_S (S2'_S and S3'_S) are stack switches, and switches S5-S6 (S5'-S6') are nMOS transistors. The capacitors C_1 (C_1')、 C_2 (C_2') and C_3 (C_3')are realized by SCDM-MOSCAPs since high

matching linearity is required. The description of AT-switch and stack switch is shown in Fig.5. In order to use AT-switch, an analog reference voltage is used: common-mode voltage $V_{cm} = \dfrac{V_{DD} + V_{SS}}{2}$ at the op amp input, the op amp output and the circuit input to maximize the signal swing. The principle of subthreshold leakage suppression scheme is similar to that presented in [6]. An extra pair of small matched capacitors C_{dg} and C'_{dg} (denoted by dashed lines) shown in Fig.6 are optional deglitching capacitors [8]. These capacitors are used to provide continuous-time feedback during the nonoverlapping times when all the switches are open and hence will eliminate the generation of output glitches. The capacitors C_{dg} and C'_{dg} are realized by SCDM-MOSCAPs since high matching linearity is required.

Fig.7 shows the op amp that is used. It is based on a fully differential folded-cascode p-type two-stage Miller-compensated configuration. The second stage is a common-source amplifier with active load which also allows a large output swing. In order to avoid the common-mode feedback (CMFB) circuit for the first stage, transistors $M51$, $M52$, $M61$, and $M62$ similar to that presented in [15] are used. For the second stage, a passive SC CMFB circuit with symmetric loading of the differential-mode loop, shown in Fig. 8 is used [3]. PCDM-MOSCAPs are used as capacitors for frequency compensation. SCDM-MOSCAPs are operated in the CMFB circuits, where matching linearity demands are high. The CMFB circuit senses the output common-mode voltage and provides the control voltage to balance the op amp's

positive and negative outputs. The CMOS transmission gates are used to connect and disconnect the common-mode sensing capacitor. For low-V_{th} process, no conductance gap appears around the middle of the supply range. The subthreshold leakage error associated with the CMOS transmission gates can be reduced effectively by choosing C_{cmfb1} larger than C_{cmfb2} with the principles similar to [1]. The unity-gain bandwidth of the op amp is simulated to be 5-MHz with a phase margin of 118º.
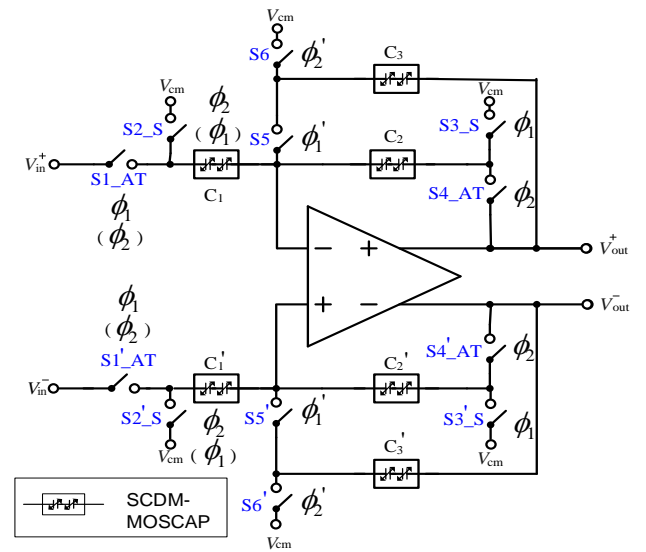

Fig. 4. MOSFET-only low-voltage S-LSCFDSCA. Depending on the input-stage clock signals, the amplifier can be either noninverting (as shown) or inverting (input-stage clocks shown in parentheses).
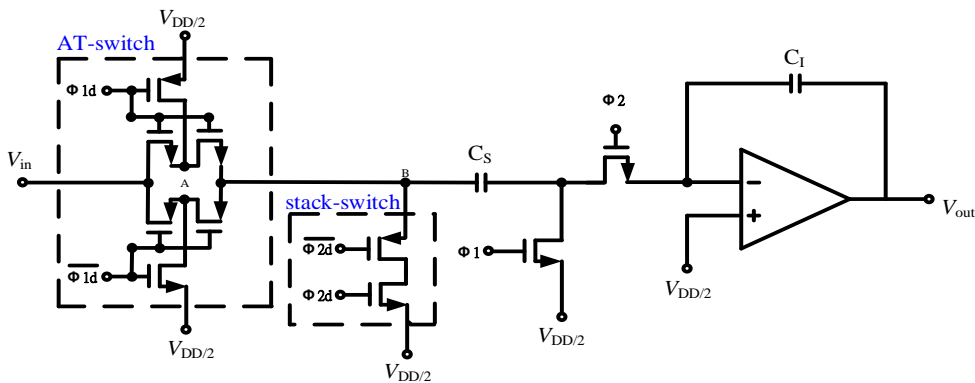

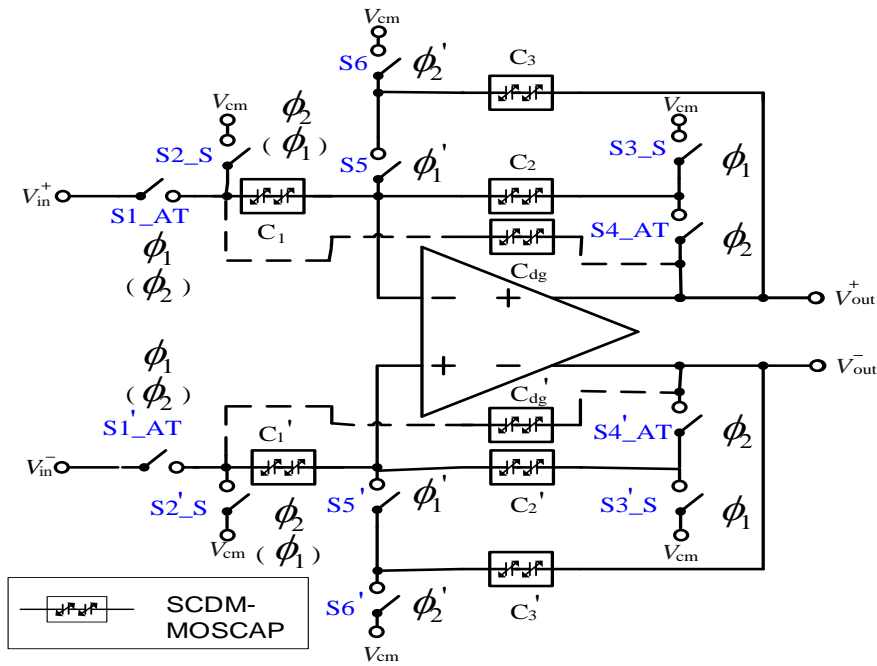**Fig. 5. AT-switch and stack switch in a SC integrator [4].**

Fig. 6. MOSFET-only low-voltage S-LSCFDSCA with matched deglitching capacitors C_{dg} and C_{dg}' to eliminate the generation of output glitches during the nonoverlapping times of the clock phases.
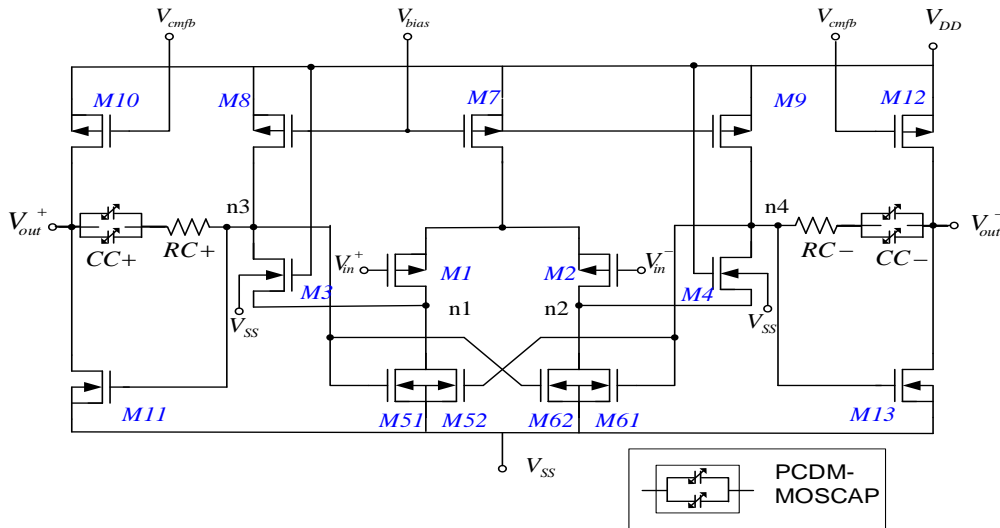

Fig. 7. Low-voltage op amp.

IV. SIMULATION and EXPERIMENTAL RESULTS

Based on the principle presented earlier, we have designed a 0.6-V MOSFET-only S-LSCFDSCA. This SC amplifier was operated with $\pm$ 0.3-V. The capacitor sizes used were C_1 (C_1') =1.25-pF, C_2 (C_2') =0.25-pF, and C_3 (C_3') =0.75-pF, for a nominal gain of -5. The circuit of Fig.6 was fabricated using a TSMC 0.18-μm CMOS technology. The threshold voltages are 0.269-V and −0.127-V for medium- V_{th} nMOS transistors and pMOS transistors, respectively.

For Fig.6, the measured (simulated) input/output waveforms for a 0.12-V peak-to-peak sinusoidal differential

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input signal are shown in Fig.9(a) (Fig.9(b)). To obtain a satisfactory settling behavior under 5-MHz unity-gain bandwidth of the op amp, the maximum clock frequency is 1-MHz. Shown in Fig.10(a) (Fig.10(b)) are the measured (simulated) input/output waveforms of a reference

switched-capacitor amplifier using MIM (metal-insulator-metal) capacitors corresponding to Fig.6. The input signal was at 10-kHz whereas the clock signal was at 1-MHz. It can be seen that the gain is very close to the nominal value of -5.
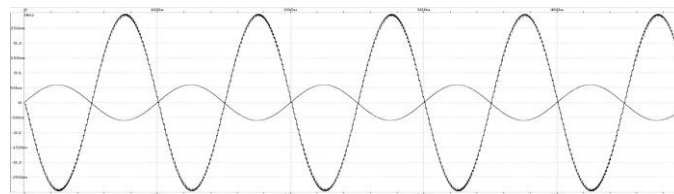

Fig. 8. Common-mode feedback circuit for the low-voltage op amp.

(a)

(b)

Fig. 9.(a) Measured and (b) simulated differential input and output waveforms of Fig. 6 (f_{clk}=1-MHz, f_{in}=10-kHz, sinusoidal differential input voltage=0.12-V_{pp}).
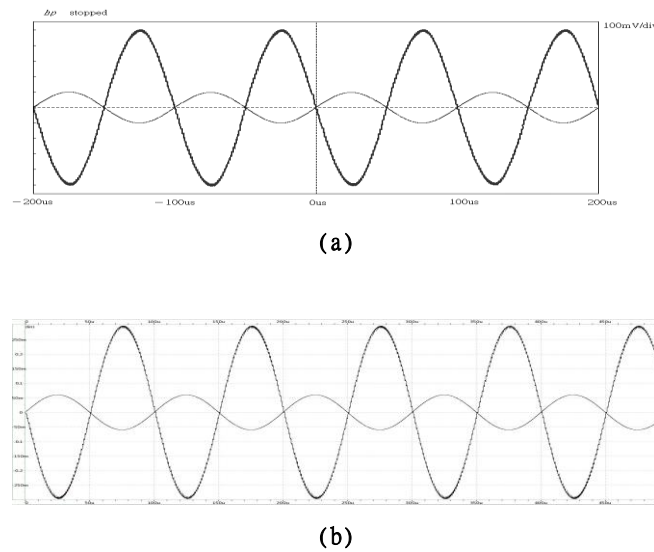
(a)

(b)

Fig. 10.(a) Measured and (b) simulated differential input and output waveforms of a reference switched-capacitor amplifier using MIM capacitors corresponding to Fig. 6(f_{clk}=1-MHz, f_{in}=10-kHz, sinusoidal differential input voltage=0.12-V_{pp}).

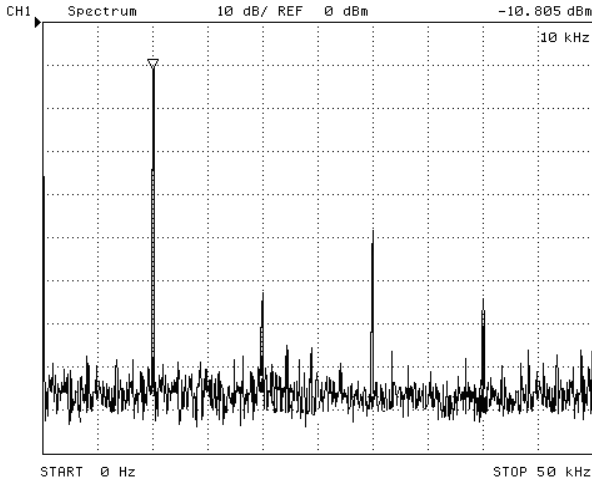**Table 1. SC amplifiers performance summary and comparison with other CMOS realization**

design	reference [7]	reference [17]	Fig.2 of reference [5]	Fig.5 of reference [5]	Fig.6 of this design	a reference switched-capacitor amplifier using MIM capacitors corresponding to Fig. 6
technology	3-μm CMOS	1.2-μm CMOS	0.35-μm CMOS	0.35-μm CMOS	0.18-μm CMOS	0.18-μm CMOS
topology	differential-to-single-ended	fully differential	fully differential	fully differential	fully differential	fully differential
clock frequency	1-MHz	16-kHz	1-MHz	1-MHz	1-MHz	1-MHz
signal-to-THD ratio	30dB@10-kHz	69dB@1-kHz	57dB@10-kHz	50dB@10-kHz	36dB@10-kHz	36dB@10-kHz
supply voltage	unknown	± 2.5-V	± 0.5-V	± 0.5-V	± 0.3-V	± 0.3-V
Power consumption	unknown	unknown	206.5-μW	206.6-μW	145.39-μW	139.19-μW

Fig.11(a) and Fig.12(a) (Fig.11(b) and Fig.12(b)) show the measured (simulated) output spectrum for a 0.12-V peak-to-peak sinusoidal differential input signal. As shown in Fig.11(a), the even-order harmonics have been largely attenuated by the fully differential topology and the largest harmonic component was 38 -dB below the fundamental of the input signal, respectively. The signal-to-THD (total harmonic distortion) ratio was 36 -dB. The circuit of Fig.6 dissipates 145.39-μW with a 0.6-V power supply. The experimental results of both S-LSCFDSCA's agree well with their simulation results. The experimental results of the proposed SC amplifier are summarized in Table.1 in comparison to other existing CMOS SC amplifiers. In the proposed MOSFET-only
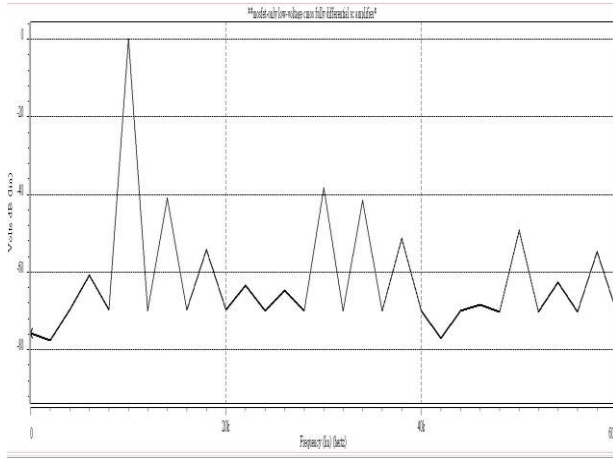
S-LSCFDSCA, the operating supply voltage is lower than those of the realizations in [17] and [5], and its signal-to-THD ratio is higher than that of the realization in [7] and lower than those of the realizations in [17] and [5] because of lower supply voltage.

The chip microphotographs of the MOSFET-only S-LSCFDSCA and the reference SC amplifier are shown in Fig.13(a) and Fig.13(b), respectively. Table.2 lists the area consumption of the MOSFET-only S-LSCFDSCA of Fig.6, in comparison to a reference SC amplifier using MIM capacitors corresponding to Fig.6. Compared to the reference SC amplifier using MIM capacitors, the MOSFET-only S-LSCFDSCA shows the almost same performance at 24% reduced area and significantly reduced processing efforts.

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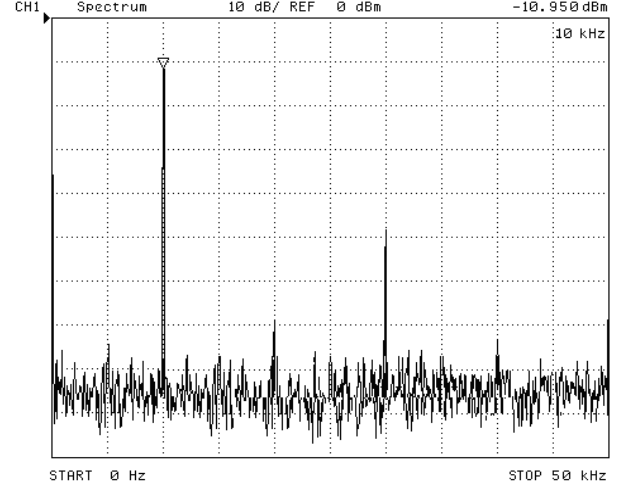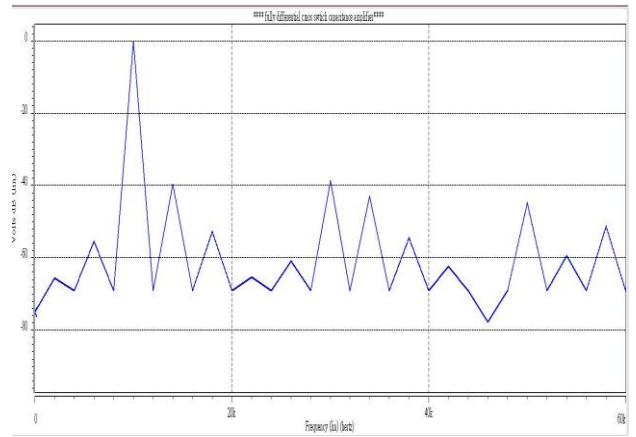

(a)

(b)

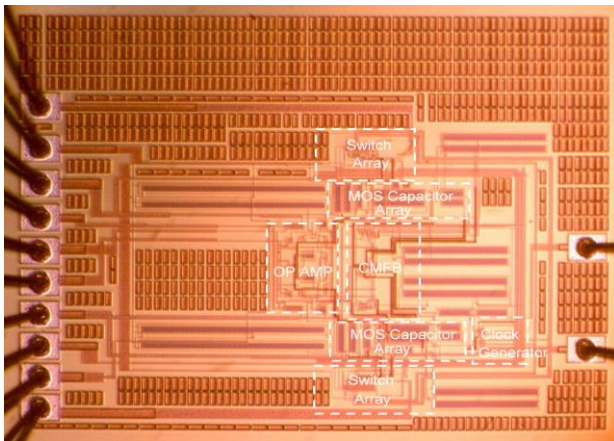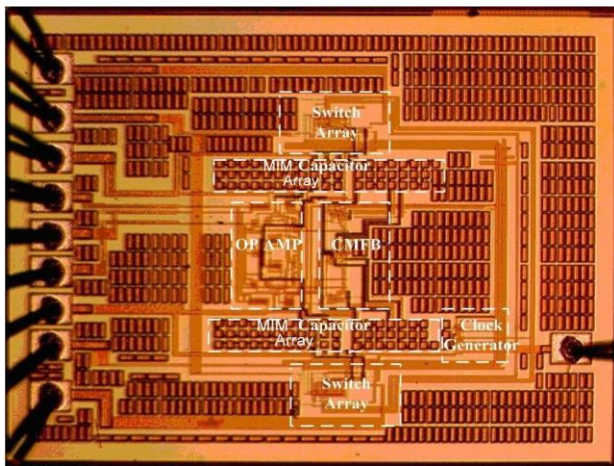**Fig. 11.(a) Measured and (b) simulated output spectrum of Fig. 6.**

(a)

(b)

Fig. 12.(a) Measured and (b) simulated output spectrum of a reference switched-capacitor amplifier using MIM capacitors corresponding to Fig.6

V. CONCLUSION

A MOSFET-only low-voltage S-LSCFDSCA has been described. The AT-switch scheme is applied to this circuit. The SC amplifier achieves 36 dB of signal-to-THD ratio for an input 10kHz sinusoidal amplitude of $0.12 V_{pp}$ and consumes 145.39-μW .The whole circuit is fabricated in a standard 0.18μm CMOS process and its chip area is 500μm ×520μm. The circuit has been implemented and all aspects of its performance have been confirmed.

(a)

(b)

Fig. 13.(a) chip microphotograph of the MOSFET-only S-LSCFDSCA and (b) chip microphotograph of the reference switched-capacitor amplifier

Table 2. Area consumption

design	Fig.6 of this design	a reference SC amplifier using MIM capacitors corresponding to Fig. 6
core area	500μm ×520μm	580μm ×590μm

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